HF TRANSCEIVER

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The transceiver presented in this article is designed to operate in the radio amateur bands of the HF frequencies (3-30MHz). It was constructed on four printed circuit boards:

- Receiver and audio amplifier
- Intermediate frequency (IF) modulator and product detector
- Up-converter mixer and radio frequency (RF) power amplifier
- Transmit / Receive (T-R) relay and RF low pass filter.

A block diagram of the transceiver is illustrated in Figure 1. In order to avoid mutual electromagnetic interferences, the receiver and IF sections are separated from the RF power stage. This requires transferring three signals between the two units; IF double-side band (DSB) modulated signal, local oscillator and the RF antenna signal.

Much effort has been directed to keep the design simple and compact by utilizing integrated circuits and direct couplings. Each of the four single-sided PCBs has its own power supply, including a voltage regulation circuitry. In its present version, the transceiver is operating in the 20m amateur band, covering 14.000-14.350MHz. The receiver can detect AM, FM and SSB signals, while the transmitter operates in a DSB mode.
I. THE RECEIVER

Figure 2 is the electronic scheme of the receiving module. The front-end of the receiver consisted of a 4.7µH inductor in series with a 27pF capacitor, constituting a resonant circuit at 14.128MHz. The two diodes at the input protect from excessive signals by clipping spikes and large amplitudes that may damage the receiver front-end. The series resonant filter it is followed by an impedance matching network.
transferring the aerial $50\Omega$ impedance into $4.5K\Omega$ input impedance of the SA605 RF stage. The matching network is shown in Figure 3.a and its transmission characteristics of the matching network are shown in Figure 3.b.

Figure 2: The receiver and product detector.

Figure 3: Front-end impedance matching network: a) scheme, b) power transmission.
The main receiving chain is based on the Philips SA605 mixer and IF system [1]. This integrated circuit (previously manufactured by Signetics with the number NE605) is a super-heterodyne receiver composing of an internal balanced mixer, local oscillator and intermediate frequency amplifiers. The 6.2V regulated supply voltage required at leg 7 is achieved by employing a zener diode.

The local oscillator (L.O.) of the SA605 is based on a varactor-tuned variable frequency oscillator (VFO). The L.O. frequency should be 455KHz below the receiving frequency, i.e. 13.545-13.895MHz. In this Colpitts configuration, the frequency is determined by the coil $L_3$, the varactor $C_V$ and the two parallel capacitors $C_{3a}$ and $C_{3b}$, as shown in Figure 4.a. The oscillation frequency of the L.O. is following the expression:

$$f_{LO}(V) = \frac{1}{2\pi \sqrt{L_3 \left[ C_V(V) + C_3 + \frac{C_1 \cdot C_2}{C_1 + C_2} \right]}}$$

While using the BB109, I found out that the coil inductance should be $L_3=0.577\mu H$ (12 turns on a T-50-6 iron powder toroid yellow core). The capacitor is approximately $C_3=150pF$ made of a $C_{3a}=120pF$ capacitor in parallel with a $C_{3b}=50pF$ trimmer (see Figure 4.a). In that case, the receiving frequency as a function of the voltage introduced to the varactor is shown in Figure 4.b. Note that besides the main 14.000-14.350MHz band (455KHz above the L.O. frequency), also image frequencies of 13.09-13.440MHz (455KHz below the L.O.) are expected to be detected as a result of a super-heterodyne configuration.

![Figure 4: The VFO: a) Resonant circuit, b) Receiving frequency as a function of the voltage in the 20m bands. The image frequencies are also shown.](image)
The continuous local oscillator sine wave appearing in leg 3 is also transferred to the up-conversion mixer in the transmitting unit of the transceiver, via a buffering 2N918 transistor in the receiver module followed by 2N2222A transistor (located in the transmitting module).

Two standard 455KHz ceramic filters are used in the IF stage. The SA605 is originally designed as an FM receiver; it includes a limiter and an FM quadrature detector, as well as an RSSI (received signal strength indicator). When an FM signal is received, the demodulated information is obtained at the unmuted audio output (leg 9). A black 455KHz standard IF transformer is used in the quadrature detection system. Appropriate design of the RSSI filter, enables also detection of AM signals. In that case the demodulated audio is obtained at the RSSI output (leg 7).

In order to detect CW or SSB transmissions, an external product detector is added. Here, a switching two-diode detector was chosen, driven by a 2N2222 bipolar transistor and an additional 455KHz black IF transformer. The detector, which in this construction is part of the IF PCB, is connected to leg 14 (the input of the SA505 limiter), where the IF signal is obtained. The 455KHz beat frequency is generated by a crystal oscillator (BFXO) in the IF board.

The audio amplifier is shown in Figure 5, including the 12V regulated power supply of the whole receiver unit. The audio amplifier is composed of the LM380 producing about 2W of RMS power over a 8Ω loudspeaker.

Figure 5: Audio amplifier and receiver 12V power supply.
II. THE IF BALANCED MODULATOR

The modulator section is based on the Motorola MC1496 balanced modulator integrated circuit [2]. Audio signals from microphone, external auxiliary line or internal tone generator are combined together by an operational amplifier TL071 (Equivalent to the 741). The microphone signal is fed to a single transistor preamplifier, enabling utilization of a standard 600Ω dynamic microphone or an electrostatic. The transistor BC149 was chosen due to its low noise performance but any other small-signal transistor will do well. The level of the microphone can be adjusted by an external potentiometer, changing the modulation level. A tone of 1,000Hz is generated by a single 2N3904 (or equivalent) transistor phase-shift oscillator, which can be switched on for transmitter testings. An internal on-board trimmer is used for setting tone modulation level. The auxiliary input impedance is 47KΩ, similar to that of standard audio inputs. The voltage gain of the TL071 audio amplifier is 20, producing 300-500mVpeak to the signal input of the balanced modulator.

The modulator generates a double-side band suppressed-carrier signal centered at an intermediate, sub-carrier frequency of 455KHz. The sub-carrier is produced by the beat frequency crystal oscillator (BFXO) based on the JFET 2N4416. The same signal is used also for the product detection in the receiver. The oscillator, is buffered by a two stage amplifier, consisting of the common emitter 2N918 followed by a common collector 2N2222. This is required in order to feed the low impedance carrier input of the balanced modulator with 60-100mVpeak of 455KHz continuous wave. A trimmer is adjusted for best carrier null the output. In order to enable CW or amplitude modulation transmission, violation of the carrier balance is created, by connecting a 1KΩ resistor from leg 4 to the ground.

The balanced modulator, 455KHz oscillator, audio preamplifier and tone generator are all constructed on the same PCB including their 12V regulated power supply.
Figure 6: Intermediate frequency balanced modulator.
III. THE UP-CONVERSION MIXER AND POWER AMPLIFIER

The unique structure of the transmitter unit shown in Figure 7, is aimed at simplification of the coupling between the mixer, driver and final amplifier. These three stages are constructed on a single PCB, installed in a separated enclosure, to minimize RF interferences to the sensitive receiver.

The up-conversion mixer is the well known SA602 double-balanced mixer and oscillator [3]. A 6.2V zener diode is employed to regulate the voltage supplied to the mixer. The double-side band, suppressed-carrier signal from the MC1496 balanced modulator (in Figure 6), is fed to the oscillator input (leg 6) of the SA602 mixer. A 455KHz ceramic band pass filter is used to reduce inter-modulation products of the sub-carrier before the up-conversion process. As mentioned before, the internal VFO of the SA605 receiver (shown in Figure 2) serves also as the local oscillator of the transmitter. The continuous sinusoidal wave of the VFO, shifted 455KHz from the transmission carrier frequency is fed to the input of the mixer (leg 1). Two RF suppressed carrier modulated signals are generated at the output ports of the balanced mixer, legs 4 and 5, with a 180° phase difference between each other. This enables a direct coupling to the subsequent push-pull driver.

The driver is based on high frequency bipolar junction transistors, the 2N3866 followed by the 2N3553. This stage is biased to operate in a class A mode, drawing a quiescent current of 80-100mA from a 12V regulated power supply. The total power dissipation at this stage is approximately 1W, requiring installation of heat sinks on the 2N3553 transistors. The switch, operating the mixer and driver, also serves as the PTT of the transmitter. The driver is coupled to the power amplifier section via a 3:1 transformer, reducing the impedance by a factor of 9 as explain in [4]. The primary supplies the voltage to the collectors of the 2N3553, while the secondary applies the bias to the gates of the MRF150 field effects transistors of the final amplifier. The transformer is made of a 22AWG enameled wires wound through a BN-43-202 ferrite core, 3 bifilar windings for the primary and a single winding for the secondary.

Two MRF150 field effects transistors (FETs) serve in the final push-pull power stage. The MRF150 transistor is an N-channel, enhancement-mode FET, designed primarily for delivering 150W, with 45% efficiency at 50V. It is often used in broad-band linear amplifiers operating in the HF band [5-8]. In the present design both gates are biased from the same regulated 5V source. The positive bias is adjusted by a 10KΩ trimmer for a quiescent current draw of 200mA from the 50V power supply. In order to avoid oscillations, two 1Ω are used, isolating the paralleling inductance, from the gates as noted in [6-7]. The power transistors should be mounted on a proper heat sink for efficient removal of the dissipated heat.
Figure 7: The up-converter and power amplifier stage a) schematics, b) photo.
IV. T/R relay and Filter

Filter calculation from
http://www.wa4dsy.net/filter/hp_lp_filter.html
V. References

1. A. K. Wong: "Reviewing key areas when designing with the SA605", Philips Semiconductors application note AN1994 (November 2007)
6. H. Granberg: "Get 600 Watts RF from four power FETs", Motorola Semiconductors application note EB104 (1983)
7. H. Granberg: "Get 600 Watts RF from four power FETs", Motorola Semiconductors application note EB104/D (1993)